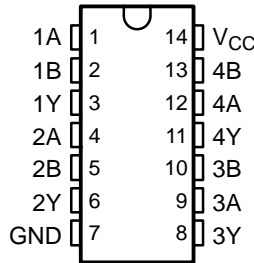


FEATURES

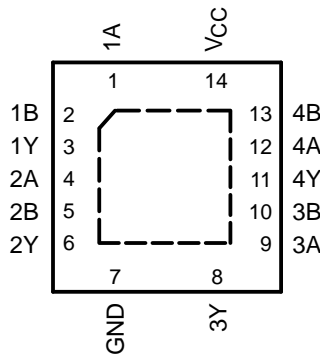
- Operate From 1.65 V to 3.6 V
- Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 3.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$

- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at $V_{CC} = 3.3 V, T_A = 25^\circ C$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

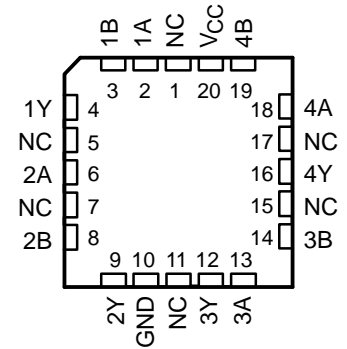
SN54LVC32A . . . J OR W PACKAGE
SN74LVC32A . . . D, DB, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC32A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC32A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

DESCRIPTION/ORDERING INFORMATION

The SN54LVC32A quadruple 2-input positive-OR gate is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC32A quadruple 2-input positive-OR gate is designed for 1.65-V to 3.6-V V_{CC} operation.

The 'LVC32A devices perform the Boolean function $Y = A + B$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LVC32ARGYR | LC32A |
| –40°C to 125°C | SOIC – D | Tube of 50 | SN74LVC32AD | LVC32A |
| | | Reel of 2500 | SN74LVC32ADR | |
| | | Reel of 250 | SN74LVC32ADT | |
| | SOP – NS | Reel of 2000 | SN74LVC32ANSR | LVC32A |
| | SSOP – DB | Reel of 2000 | SN74LVC32ADBR | LC32A |
| | TSSOP – PW | Tube of 90 | SN74LVC32APW | LC32A |
| Reel of 2000 | | SN74LVC32APWR | | |
| Reel of 250 | | SN74LVC32APWT | | |
| –55°C to 125°C | CDIP – J | Tube of 25 | SNJ54LVC32AJ | SNJ54LVC32AJ |
| | CFP – W | Tube of 150 | SNJ54LVC32AW | SNJ54LVC32AW |
| | LCCC – FK | Tube of 55 | SNJ54LVC32AFK | SNJ54LVC32AFK |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

**FUNCTION TABLE
 (EACH GATE)**

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | X | H |
| X | H | H |
| L | L | L |

LOGIC DIAGRAM, EACH GATE (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|------------------|---|---|-----------------------|------|------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V | |
| V _I | Input voltage range ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Output voltage range ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 | mA |
| I _O | Continuous output current | | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | | ±100 | mA |
| θ _{JA} | Package thermal impedance | D package ⁽⁴⁾ | | 86 | °C/W |
| | | DB package ⁽⁴⁾ | | 96 | |
| | | NS package ⁽⁴⁾ | | 76 | |
| | | PW package ⁽⁴⁾ | | 113 | |
| | | RGY package ⁽⁵⁾ | | 47 | |
| T _{stg} | Storage temperature range | -65 | 150 | °C | |
| P _{tot} | Power dissipation | T _A = -40°C to 125°C ⁽⁶⁾⁽⁷⁾ | | 500 | mW |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.
- (6) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (7) For the DB, DGV, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVC32A | | UNIT | | |
|-----------------|------------------------------------|----------------------------------|-----|------|-----------------|------|
| | | | | | –55 TO 125°C | |
| | | MIN | MAX | | | |
| V _{CC} | Supply voltage | Operating | | 2 | 3.6 | V |
| | | Data retention only | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 2 | | V |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7 V to 3.6 V | | 0.8 | | V |
| V _I | Input voltage | | | 0 | 5.5 | V |
| V _O | Output voltage | | | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2.7 V | | –12 | | mA |
| | | V _{CC} = 3 V | | –24 | | |
| I _{OL} | Low-level output current | V _{CC} = 2.7 V | | 12 | | mA |
| | | V _{CC} = 3 V | | 24 | | |
| Δt/Δv | Input transition rise or fall rate | | | 7 | | ns/V |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Recommended Operating Conditions⁽¹⁾

| | | SN74LVC32A | | | | | | UNIT | | |
|-----------------|------------------------------------|------------------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------------------------|-----------------|------|
| | | T _A = 25°C | | –40 TO 85°C | | –40 TO 125°C | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | | | |
| V _{CC} | Supply voltage | Operating | | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | | 1.5 | | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 1.7 | | 1.7 | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 2 | | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | 0.7 | | 0.7 | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | | 0.8 | | 0.8 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | –4 | | –4 | | –4 | | mA |
| | | V _{CC} = 2.3 V | | –8 | | –8 | | –8 | | |
| | | V _{CC} = 2.7 V | | –12 | | –12 | | –12 | | |
| | | V _{CC} = 3 V | | –24 | | –24 | | –24 | | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | 4 | | 4 | | 4 | | mA |
| | | V _{CC} = 2.3 V | | 8 | | 8 | | 8 | | |
| | | V _{CC} = 2.7 V | | 12 | | 12 | | 12 | | |
| | | V _{CC} = 3 V | | 24 | | 24 | | 24 | | |
| Δt/Δv | Input transition rise or fall rate | 7 | | 7 | | 7 | | 7 | | ns/V |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54LVC32A, SN74LVC32A QUADRUPLE 2-INPUT POSITIVE-OR GATES

SCAS286P–JANUARY 1993–REVISED APRIL 2005

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | SN54LVC32A | | UNIT |
|-----------------|---|----------------|----------------|-----|---------|
| | | | –55 TO 125°C | | |
| | | | MIN | MAX | |
| V_{OH} | $I_{OH} = -100 \mu A$ | 2.7 V to 3.6 V | $V_{CC} - 0.2$ | | V |
| | $I_{OH} = -12 \text{ mA}$ | 2.7 V | 2.2 | | |
| | $I_{OH} = -24 \text{ mA}$ | 3 V | 2.4 | | |
| V_{OL} | $I_{OL} = 100 \mu A$ | 2.7 V to 3.6 V | 0.2 | | V |
| | $I_{OL} = 12 \text{ mA}$ | 2.7 V | 0.4 | | |
| | $I_{OL} = 24 \text{ mA}$ | 3 V | 0.55 | | |
| I_I | $V_I = 5.5 \text{ V}$ or GND | 3.6 V | ± 5 | | μA |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 3.6 V | 10 | | μA |
| ΔI_{CC} | One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND | 2.7 V to 3.6 V | 500 | | μA |

Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | SN74LVC32A | | | | | | UNIT | |
|-----------------|---|-----------------|--------------------|-----|-----|----------------|-----|----------------|------|---------|
| | | | $T_A = 25^\circ C$ | | | –40 TO 85°C | | –40 TO 125°C | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| V_{OH} | $I_{OH} = -100 \mu A$ | 1.65 V to 3.6 V | $V_{CC} - 0.2$ | | | $V_{CC} - 0.2$ | | $V_{CC} - 0.3$ | | V |
| | $I_{OH} = -4 \text{ mA}$ | 1.65 V | 1.29 | | | 1.2 | | 1.05 | | |
| | $I_{OH} = -8 \text{ mA}$ | 2.3 V | 1.9 | | | 1.7 | | 1.55 | | |
| | $I_{OH} = -12 \text{ mA}$ | 2.7 V | 2.2 | | | 2.2 | | 2.05 | | |
| | | 3 V | 2.4 | | | 2.4 | | 2.25 | | |
| V_{OL} | $I_{OL} = 100 \mu A$ | 1.65 V to 3.6 V | | | | 0.1 | | 0.2 | | V |
| | $I_{OL} = 4 \text{ mA}$ | 1.65 V | | | | 0.24 | | 0.45 | | |
| | $I_{OL} = 8 \text{ mA}$ | 2.3 V | | | | 0.3 | | 0.7 | | |
| | $I_{OL} = 12 \text{ mA}$ | 2.7 V | | | | 0.4 | | 0.6 | | |
| | $I_{OL} = 24 \text{ mA}$ | 3 V | | | | 0.55 | | 0.55 | | |
| I_I | $V_I = 5.5 \text{ V}$ or GND | 3.6 V | | | | ± 1 | | ± 5 | | μA |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 3.6 V | | | | 1 | | 10 | | μA |
| ΔI_{CC} | One input at $V_{CC} - 0.6 \text{ V}$, Other inputs at V_{CC} or GND | 2.7 V to 3.6 V | | | | 500 | | 500 | | μA |
| C_i | $V_I = V_{CC}$ or GND | 3.3 V | | | | 5 | | | | pF |

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | SN54LVC32A | | UNIT |
|-----------|--------------|-------------|-------------------|--------------|-----|------|
| | | | | –55 TO 125°C | | |
| | | | | MIN | MAX | |
| t_{pd} | A or B | Y | 2.7 V | 4.4 | | ns |
| | | | 3.3 V \pm 0.3 V | 1 | 3.8 | |

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

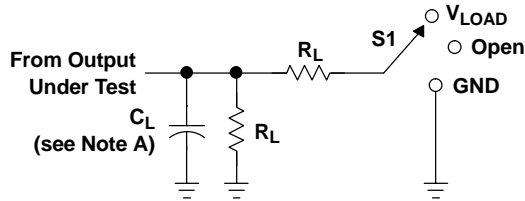
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | SN74LVC32A | | | | | | UNIT | |
|--------------------|-----------------|----------------|-----------------|-----------------------|-----|-----|-------------|-----|--------------|------|-----|
| | | | | T _A = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| t _{pd} | A or B | Y | 1.8 V ± 0.15 V | 1 | 4.2 | 8.2 | 1 | 8.7 | 1 | 10.2 | ns |
| | | | 2.5 V ± 0.2 V | 1 | 2.6 | 4.9 | 1 | 5.4 | 1 | 6.9 | |
| | | | 2.7 V | 1 | 3 | 4.2 | 1 | 4.4 | 1 | 5.5 | |
| | | | 3.3 V ± 0.3 V | 1 | 2.5 | 3.6 | 1 | 3.8 | 1 | 5 | |
| t _{sk(o)} | | | 3.3 V ± 0.3 V | | | | | 1 | 1.5 | ns | |

Operating Characteristics

T_A = 25°C

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|-----------------|--|--------------------|-----------------|------|------|
| C _{pd} | Power dissipation capacitance per gate | f = 10 MHz | 1.8 V | 7.5 | pF |
| | | | 2.5 V | 10.6 | |
| | | | 3.3 V | 12.5 | |

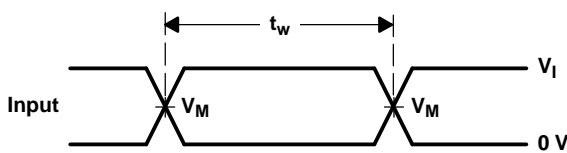
PARAMETER MEASUREMENT INFORMATION



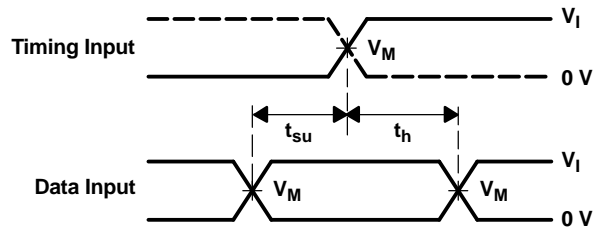
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

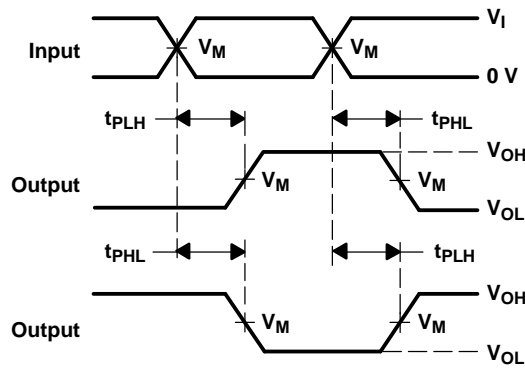
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



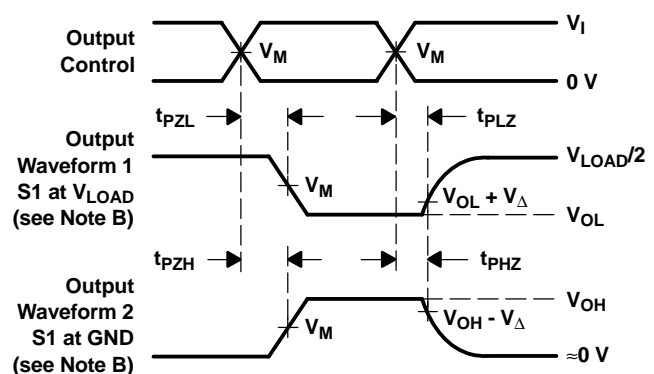
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9761801Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| 5962-9761801QCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 5962-9761801QDA | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74LVC32AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADBLE | OBSOLETE | SSOP | DB | 14 | | TBD | Call TI | Call TI |
| SN74LVC32ADBR | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADBRG4 | ACTIVE | SSOP | DB | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADT | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADTE4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ADTG4 | ACTIVE | SOIC | D | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ANSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWE4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWLE | OBSOLETE | TSSOP | PW | 14 | | TBD | Call TI | Call TI |
| SN74LVC32APWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWRE4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWT | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32APWTE4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74LVC32APWTG4 | ACTIVE | TSSOP | PW | 14 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVC32ARGYR | ACTIVE | QFN | RGY | 14 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SN74LVC32ARGYRG4 | ACTIVE | QFN | RGY | 14 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| SNJ54LVC32AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type |
| SNJ54LVC32AJ | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| SNJ54LVC32AW | ACTIVE | CFP | W | 14 | 1 | TBD | A42 | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LVC32A, SN74LVC32A :

- Automotive: [SN74LVC32A-Q1](#)
- Enhanced Product: [SN74LVC32A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC32ADBR | SSOP | DB | 14 | 2000 | 330.0 | 16.4 | 8.2 | 6.6 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC32ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LVC32ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC32APWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 7.0 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC32ARGYR | QFN | RGY | 14 | 1000 | 180.0 | 12.4 | 3.85 | 3.85 | 1.35 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC32ADBR | SSOP | DB | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LVC32ADR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN74LVC32ANSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74LVC32APWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| SN74LVC32ARGYR | QFN | RGY | 14 | 1000 | 190.5 | 212.7 | 31.8 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



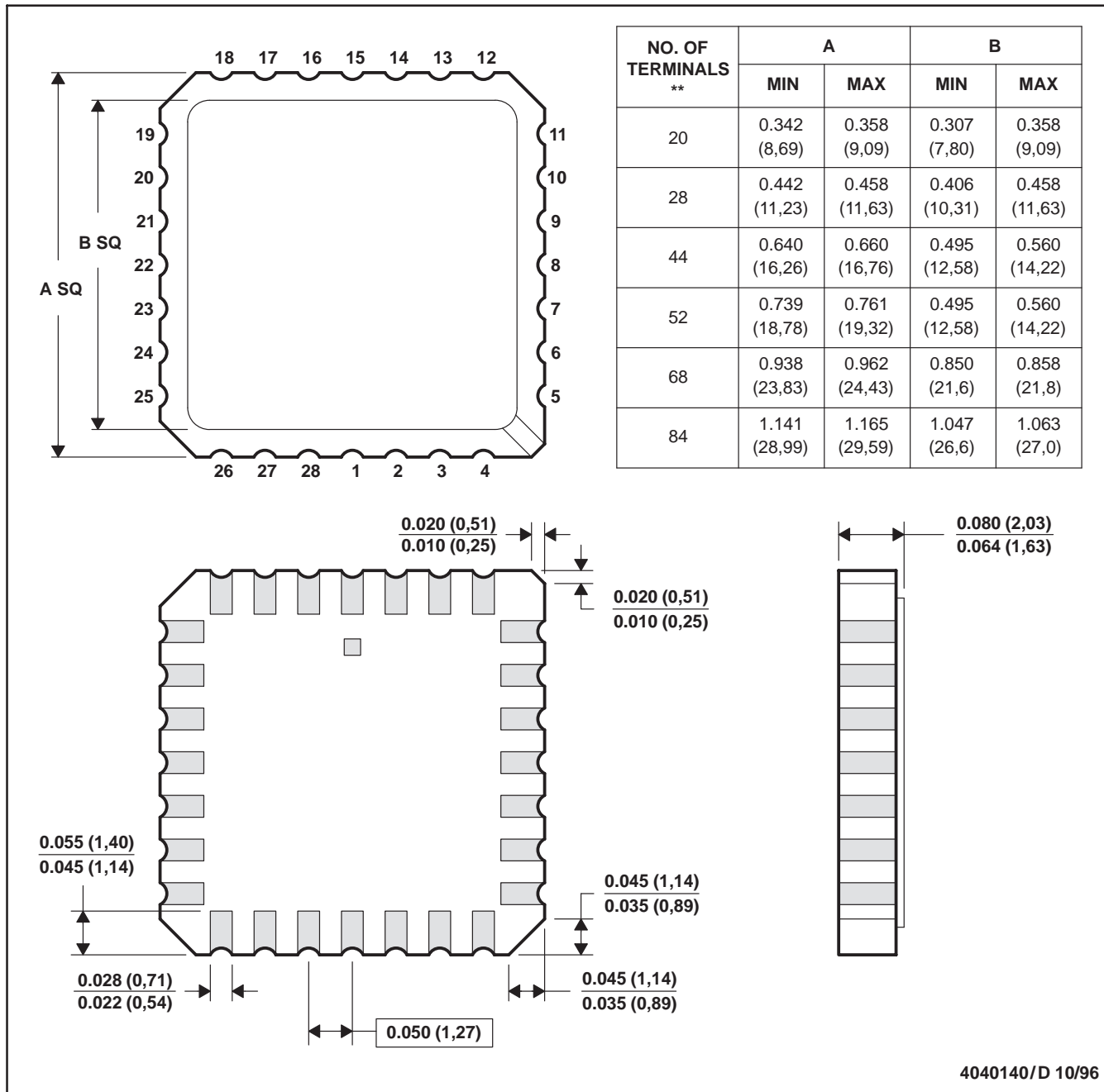
4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

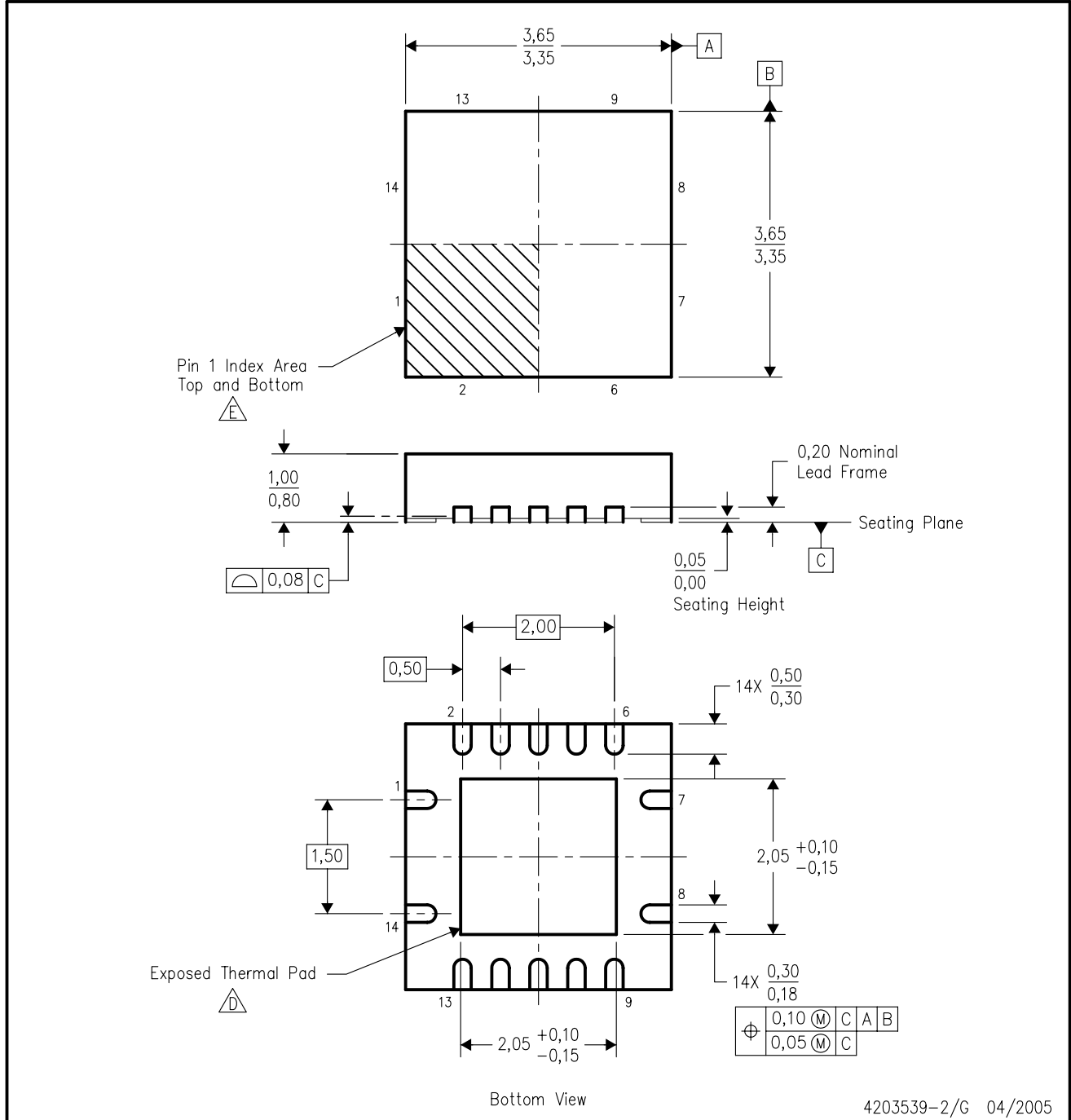
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



4203539-2/G 04/2005

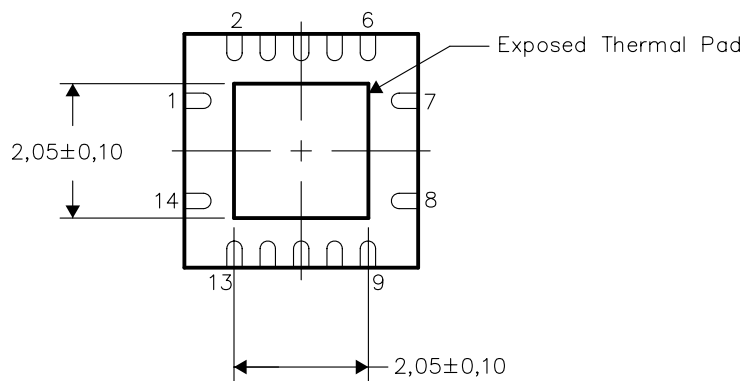
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - F. Package complies to JEDEC MO-241 variation BA.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

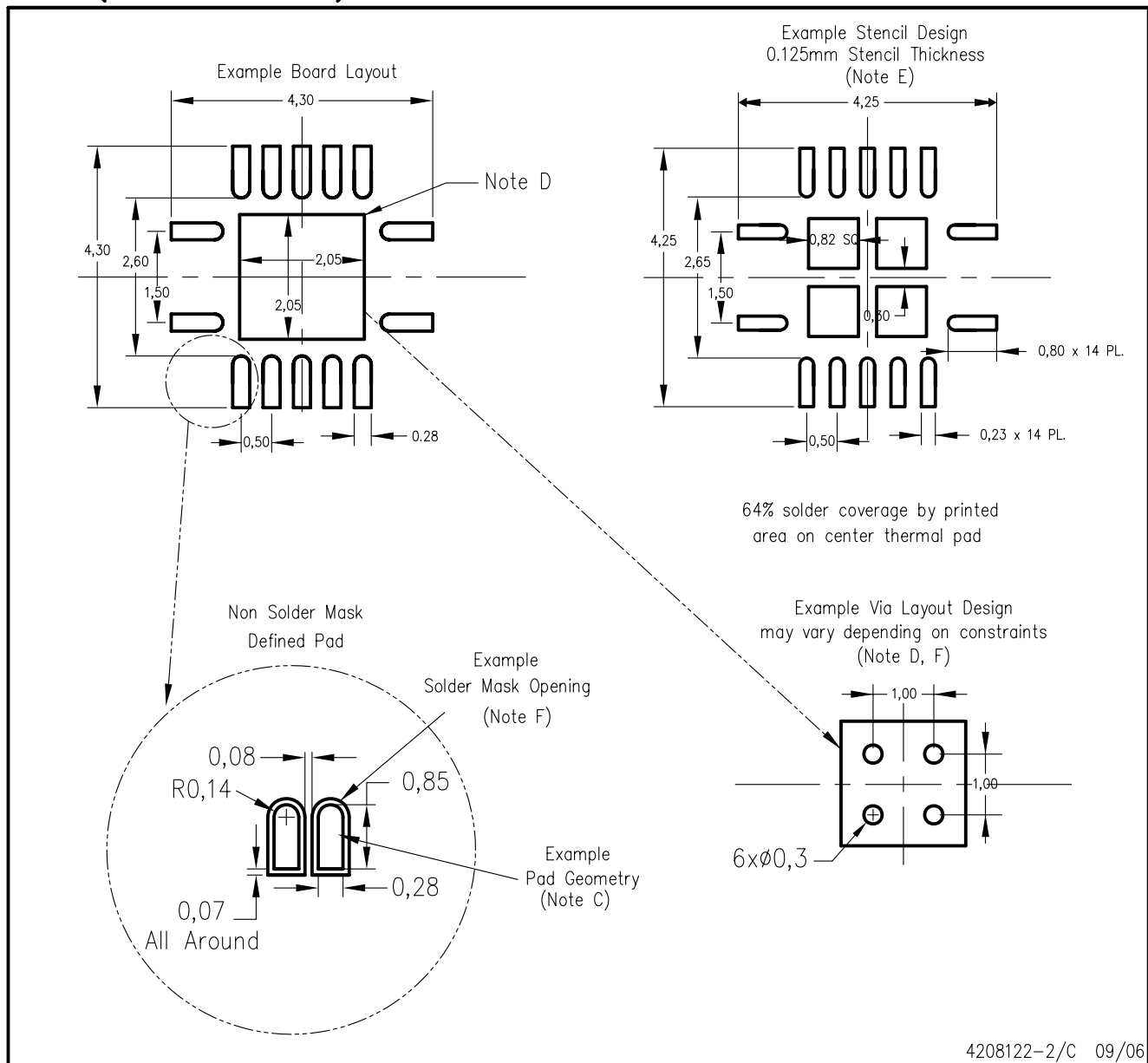


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGY (R-PQFP-N14)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

W (R-GDFP-F14)

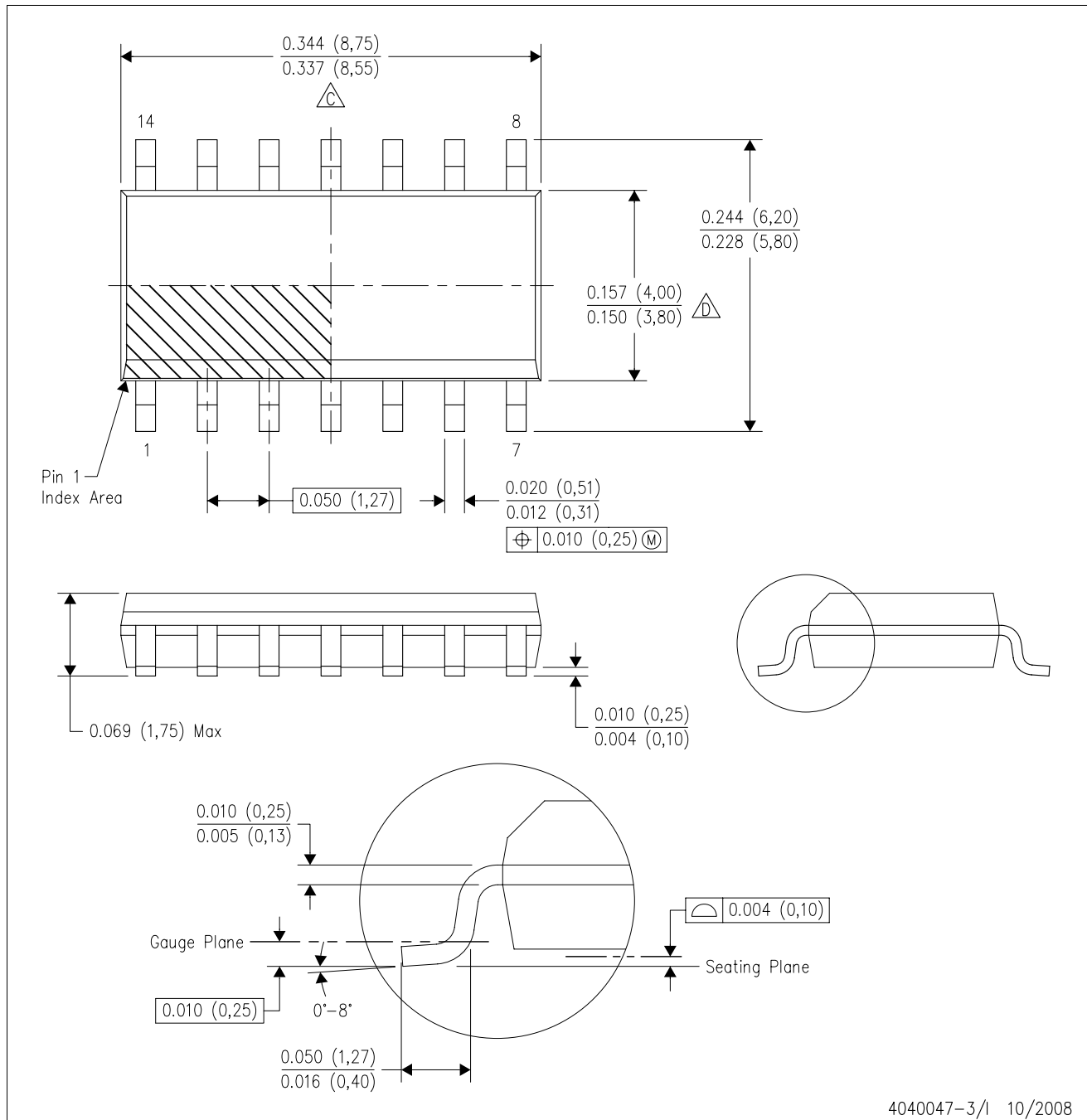
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AB.

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